#6 SP 01-12-04

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Seongmoon WANG

Appln. No.: 09/805,899

Confirmation No.: 3488

Filed: March 15, 2001

Docket No: A7936

Group Art Unit: 2133

Examiner: Shelly A. CHASE

For: LOW HARDWARE OVERHEAD SCAN BASED 3-WEIGHT WEIGHTED RANDOM BIST ARCHITECTURES

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §§ 1.97 and 1.98

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure under 37 C.F.R. § 1.56, Applicant hereby notifies the U.S. Patent and Trademark Office of the documents which are listed on the attached PTO/SB/08 A & B (modified) form and/or listed herein and which the Examiner may deem material to patentability of the claims of the above-identified application.

One copy of each of the listed documents is submitted herewith.

1. M. Abramovici, M. A. Breuer, and A. D. Friedman. *Digital Systems Testing and Testable Design*. Computer Science Press, New York, N.Y., 1990.

2. M. F. AlShaibi and C. R. Kime. MFBIST: A BIST Method for Random Pattern Resistant Circuits. In *Proceedings IEEE International Test Conference,* pages 176-185, 1996.

3. M. Bershteyn. Calculation of Multiple Sets of Weights for Weighted Random Testing. In *Proceedings IEEE International Test Conference*, pages 1031-1040, 1993.

4. P. H. B., W. H. McAnney, and J. Savir. *Built-In Test for VLSI: Pseudorandom Techniques*. John Wiley & Sons, 1987.

5. D. E. Goldberg. *Genetic Algorithms in Search, Optimization, and Machine Learning*. Addison Wesley, Reading, M.A., 1989.

6. J. Hartmann and G. Kemnitz. How to Do Weighted Random Testing for BIST. In *Proceedings IEEE International Conference on Computer-Aided Design*, pages 568-571, 1993.

7. J. H. Holland. *Adaptation in Natural and Artificial Systems*. University of Michigan Press, Ann Arbor, M.I., 1975.

8. M. Karkala, N A. Touba, and H.-J. Wunderlich. Special ATPG to Correlate Test Patterns for Low-Overhead Mixed-Mode BIST. In *In proceedings 7yrd Asian Test Symposium*, 1998.

9. S. Pateras and J. Rajski. Cube-Contained Random Patterns and Their Application to the Complete Testing of Synthesized Multi-level Circuits. In *Proceedings IEEE International Test Conference*, pages 473-482, 1991.

10. I. Pomeranz and S. Reddy. 3-Weight Pseudo-Random Test Generation Based on a Deterministic Test Set for Combinational and Sequential Circuits. *IEEE Trans. On Computer-Aided Design of Integrated Circuit and System*, Vol. 12:1050-1058, July 1993.

11. N. Touba and E. McCluskey. Synthesis of Mapping Logic for Generating Transformed Pseudo-Random Patterns for BIST. In *Proceedings IEEE International Test Conference*, pages 674-682, 1995.

12. N. A. Touba and E. J. McCluskey. Altering a Pseudo-Random Bit Sequence for Scan-Based BIST. In Proceedings *IEEE International Test Conference*, pages 167-175, 1996.

13. H.-J. Wunderlich and G. Kiefer. Bit-Flipping BIST. In *Proceedings VLSI Testing Symposium*, pages 337-343, 1996.

14. H.-J. Wunderlich. Multiple Distributions for Biased Random Test Patterns. In *Proceedings IEEE International Test Conference*, pages 236-244, 1988.

15. S. Hellebrand. B. Reeb. S. Tarnick. H.-J. Wunderlich. Pattern Generation for a Deterministic BIST Scheme. In *Proceedings IEEE International Test Conference*, pages 88-94, 1995.

16. J. A. Waicukauski. E. Lindbloom. E. B. Eichelberger. O. P. Forlenza. A method for generating weighted random test patterns. IBM J. Res. Develop. Vol. 33. No. 2 March 1989, pages 149-161.

17. G. Kiefer and H.-J. Wunderlich. Using BIST Control for Pattern Generation. In *Proceedings IEEE International Test Conference*, pages 347-355, 1997.

18. J. L. Hennessy and David A. Patterson. Computer Organization and Design.

19. On-Chip Bus Attributes. Specification 1 Version 1.0 (OCB 1 1.0) dated August 1998, On-Chip Bus Development Working Group, VSI Alliance.

20. B. Reeb and H.-J. Wunderlich. Deterministic Pattern Generation for Weighted Random Pattern Testing. In *Proceedings IEEE International Test Conference*, pages 30-36, 1996.

21. Y. Savaria. B. Lague. B. Kaminska. A Fragmatic Approach to the Design of Self-Testing Circuits. Electrical Engineering Dept., Ecole Polytechnique de Montreal. In *Proceedings IEEE International Test Conference*, pages 745-754, 1989.

22. H.-C. Tsai. K.-T. Cheng. C.-J. Lin. S. Bhawmik. Efficient Test-Point Selection for Scan-Based BIST. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 6, No. 4, December 1998.

23. N. Tamarapalli and Janusz Rajski. Constructive Multi-Phase Test Point Insertion for Scan-Based BIST. In *Proceedings IEEE International Test Conference*, pages 649-658, 1996.

The present Information Disclosure Statement is being filed in response to a request for information under 37 C.F.R 1.105 made in the Office Action dated September 5, 2003. As noted in item 5 of the request, the Examiner has waived the fee and the certification requirement. Therefore no fee or statement is included.

The submission of the listed documents is not intended as an admission that any such document constitutes prior art against the claims of the present application. Applicant does not waive any right to take any action that would be appropriate to antedate or otherwise remove any listed document as a competent reference against the claims of the present application.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account. A duplicate copy of this paper is attached.

Respectfully submitted,

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